REMARKS

The Examiner has rejected Claims 1-30 under 35 U.S.C. 101 as being directed towards non-statutory subject matter. Such rejection is deemed avoided by virtue of the amendments made hereinabove to the independent claims.

The Examiner has rejected Claims 1-12, 18-21, 24-27, 28, and 30 under 35 U.S.C. 103(a) as being unpatentable over Rivard et al. (U.S. Patent No. 5,987,567). In addition, the Examiner has rejected Claims 13-17, 22, 23, and 29 under 35 U.S.C. 103(a) as being unpatentable over Rivard, in view of Applicant Admitted Prior Art (AAPA). Applicant respectfully disagrees with such rejections.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*,947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

With respect to the first element of the prima facie case of obviousness, the Examiner has argued that "Rivard teaches that memory data [is] associated with instructions" and "[i]t would have been obvious... to incorporate instructions and data [of] Col. 7, lines 3-6 into the sending data of Col. 6, lines 50-60 because [the] combination of instruction and data would provide a constant latency which includes time for exiting and reentering the graphic pipeline. see col.7, lines 1-3." To the contrary, applicant respectfully asserts that it would not have been obvious to modify the teaching of Rivard, especially in view of the vast evidence to the contrary.

Applicant respectfully points out that Rivard teaches that "[b]ecause memory request generator 1020 is between cache tag blocks 1010, 1015 and cache data store 1030, generator 1020 can perform DRAM 655 memory requests before the address and instruction information reach cache data store and memory data resolver 1030" (Col. 6, lines 62-66 - emphasis added). In addition, Rivard teaches that "[o]nce memory requests are generated, there is, depending on the DRAM design, a constant latency of about five to ten clock cycles (or possibly more) which includes time for exiting and reentering the graphics pipeline hardware, to effect a page hit" and "[t]herefore, graphics accelerator system 635 includes pipeline latency elements 1025 to coordinate arrival of the memory data and of the associated instructions at cache data store and memory data resolver 1030" (Col. 6, line 66-Col. 7, line 7 - emphasis added). Furthermore, Rivard discloses that "the memory request generator is coupled between the cache tag block and the cache data store for performing a memory request before an address and instruction information associated with the needed texels reach the cache data store" (Col. 10, lines 48-52 - emphasis added).

Applicant respectfully asserts that a combination of data and instructions in Rivard, as suggested by the Examiner, would result in no need for the purposefully included "pipeline latency elements" of Rivard since the combination of data and instructions would arrive together. As a result, there is no suggestion that the modification of the Rivard reference, as claimed by the Examiner, is desired. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." 916 F.2d at 682, 16 USPQ2d at 1432.).

Additionally, applicant respectfully notes that modifying the Rivard reference, as suggested by the Examiner, would change the principle of operation of the Rivard system, since it would obviate the need for the purposefully included "pipeline latency

elements 1025," as noted above. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)

Furthermore, applicant respectfully asserts that, in the Abstract, Rivard teaches "[a] system for caching texel information in a cache data store, for use in a graphics rendering system which uses interpolative sampling to compute texture color values." Additionally, Rivard teaches that "[t]he system includes a texel memory storing texel information, a graphics application program for using interpolative sampling to compute dynamic texture values, a first cache data storage for a number of the most-recently-retrieved texels, a second cache data storage for a previously-retrieved adjacent line of texels, cache tag blocks for determining whether the texels needed by the graphics accelerator system are cached in either of the first or second cache data stores, and a memory request generator for retrieving texels from texel memory upon indication of a miss by the cache tag blocks."

However, Rivard does not recognize one of the various possible problems solved by applicant, namely to "accommodate the programmability of recent texture and shader modules without being inhibited by the size of associated programs," for example. It was this insight in solving this problem that helped the inventors conceive of the claimed invention which overcomes the drawbacks of the prior art. "Because that insight was contrary to the understandings and expectations of the art, the structure effectuating it would not have been obvious to those skilled in the art." *Schenck v. Nortron Corp.*, 713 F.2d at 785, 218 USPQ at 700 (citations omitted).

Additionally, applicant respectfully asserts that the following excerpts from Rivard demonstrate that such reference, in fact, *teaches away* from applicant's claimed invention.

> "If the interface to DRAM 655 is 32-bits wide, the texture mode indicates a 16-bit per pixel texture lookup and the data is

conveniently aligned in the texture map, then it is possible to satisfy two lookup requests with a single read request. However, if the data is not aligned, then two read requests are needed." (Col. 6, lines 56-61 - emphasis added)

"Therefore, graphics accelerator system 635 includes pipeline latency elements 1025 to coordinate arrival of the memory data and of the associated instructions at cache data store and memory data resolver 1030." (Col. 7, lines 3-7 - emphasis added)

"...the memory request generator is coupled between the cache tag block and the cache data store for performing a memory request before an address and instruction information associated with the needed texels reach the cache data store." (Col. 10, lines 48-52 - emphasis added)

Applicant respectfully asserts that the "pipeline latency elements 1025," as described in Rivard, are introduced specifically "to coordinate arrival of the memory data and of the associated instructions at cache data store and memory data resolver 1030" (emphasis added). Thus, Rivard actually *teaches away* from applicant's claim language by intentionally incorporating the "pipeline latency elements 1025" for the specific purpose of coordinating the arrival of the instructions and the memory data from separate sources. A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, *teaches away* from the claimed invention. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

Thus, clearly at least the first element of the *prima facie* case of obviousness has not been met by the Rivard reference.

More importantly, with respect to the third element of the *prima facie* case of obviousness, applicant respectfully asserts that the Rivard reference also fails to meet all of applicant's claim limitations. Specifically, with respect to independent Claims 1, 24-27, and 30, the Examiner has relied on Figure 6 and Figure 10, in addition to the following excerpt from Rivard to make a prior art showing of applicant's claimed "sending an instruction request to video memory, where a texture module in a graphics pipeline sends the instruction request to the video memory" (see this or similar, but not necessarily identical language in the foregoing independent claims).

"...Memory request generator 1020 generates memory requests for all misses (up to four for bi-linear sampling and up to eight for tri-linear sampling), and forwards the requests to DRAM 655 for information retrieval. DRAM 655 returns the memory data on bus 660 to cache data store and memory data resolver 1030, which stores the memory data at the..." (Col. 6, lines 50-55 - emphasis added)

Applicant respectfully asserts that the figures relied on by the Examiner only generally illustrate a computer system and a block diagram detailing the graphics accelerator system showing the pipeline latency elements 1025. In addition, the excerpt relied on by the Examiner merely teaches that the "[m]emory request generator 1020 generates memory requests for all misses (up to four for bi-linear sampling and up to eight for tri-linear sampling), and forwards the requests to DRAM 655 for information retrieval" (emphasis added). However, disclosing that a memory request is generated for all misses fails to teach "sending an instruction request to memory utilizing a texture module in a graphics pipeline" (emphasis added), as claimed by applicant.

Furthermore, applicant respectfully asserts that the following excerpts from Rivard further demonstrate that the Rivard fails to disclose applicant's claimed "sending an instruction request to video memory, where a texture module in a graphics pipeline sends the instruction request to the video memory" (see this or similar, but not necessarily identical language in the foregoing independent claims).

"If the interface to DRAM 655 is 32-bits wide, the texture mode indicates a 16-bit per pixel texture lookup and the data is conveniently aligned in the texture map, then it is possible to satisfy two lookup requests with a single read request. However, if the data is not aligned, then two read requests are needed." (Col. 6, lines 56-61 - emphasis added)

"Therefore, graphics accelerator system 635 includes pipeline latency elements 1025 to coordinate arrival of the memory data and of the associated instructions at cache data store and memory data resolver 1030." (Col. 7, lines 3-7 - emphasis added)

"...the memory request generator is coupled between the cache tag block and the cache data store for performing a memory request before an address and instruction information associated with the needed texels reach the cache data store." (Col. 10, lines 48-52 - emphasis added)

First, applicant respectfully points out that Rivard merely teaches that "the memory request generator is coupled between the cache tag block and the cache data store for performing a memory request before an address and instruction information associated with the needed texels reach the cache data store" (emphasis added). Clearly, coordinating the arrival of "memory data", where "the data is conveniently aligned in the texture map" (emphasis added), as in Rivard (see excerpts above), fails to teach "sending an instruction request" (emphasis added), as claimed by applicant.

Second, applicant respectfully asserts that Rivard simply discloses that a memory request is performed before an address and instruction information associated with the needed texels reach the cache data store (see excerpts above). Thus, the memory data in Rivard simply relates to texel data, which clearly fails to suggest "sending an instruction request to memory utilizing a texture module in a graphics pipeline" (emphasis added), as claimed by applicant.

Additionally, with respect to independent Claims 1, 24-27, and 30, the Examiner has relied on Figures 6 and 10, along with Col. 6 lines 53-55 from Rivard (see below) to make a prior art showing of applicant's claimed "receiving instructions from the video memory in response to the instruction request utilizing the texture module in the graphics pipeline" (see this or similar, but not necessarily identical language in the foregoing independent claims).

> "...to DRAM 655 for information retrieval. DRAM 655 returns the memory data on bus 660 to cache data store and memory data resolver 1030, which stores the memory data at the..." (Col. 6, lines 53-55)

Applicant respectfully asserts that the figures relied on by the Examiner only generally illustrate a computer system and a block diagram detailing the graphics accelerator system showing the pipeline latency elements 1025. In addition, the excerpt relied on by the Examiner merely teaches that "DRAM 655 returns the memory data on bus 660 to cache data store and memory data resolver 1030" (emphasis added). However, merely returning memory data to a cache data store fails to teach "receiving

instructions from the video memory in response to the instruction request utilizing the texture module in the graphics pipeline" (emphasis added), as claimed by applicant.

Furthermore, as mentioned above, Rivard teaches that "[i]f the interface to DRAM 655 is 32-bits wide, the texture mode indicates a 16-bit per pixel texture lookup and the data is conveniently aligned in the texture map, then it is possible to satisfy two lookup requests with a single read request" (emphasis added). Additionally, Rivard discloses that "the memory request generator is coupled between the cache tag block and the cache data store for performing a memory request before an address and instruction information associated with the needed texels reach the cache data store" (emphasis added). Clearly, coordinating the arrival of "memory data", where "the data is conveniently aligned in the texture map" (emphasis added), as in Rivard, fails to even suggest "receiving instructions from the video memory in response to the instruction request" (emphasis added), as claimed by applicant. Additionally, disclosing that a memory request is performed before an address and instruction information associated with the needed texels reach the cache data store, fails to disclose "receiving instructions from the video memory in response to the instruction request utilizing the texture module in the graphics pipeline" (emphasis added), as claimed by applicant, and actually *teaches away* from applicant's claimed invention.

Moreover, with respect to independent Claim 28, the Examiner has relied on Figure 6 and Col. 6, lines 48-52 in Rivard to make a prior art showing of applicant's claimed "sending an instruction request to video memory, where the texture module sends the instruction request to the video memory."

Applicant again respectfully asserts that Figure 6 only shows a block diagram of a computer system, and that the excerpt relied on by the Examiner simply discloses that "the cache tag blocks 1010 and 1015 forward a cache write address to memory request generator 1020" where "[m]emory request generator 1020 generates memory requests for all misses." Clearly, generating a memory request for all misses, as in Rivard, does not meet applicant's claimed "sending an instruction request" (emphasis added), as claimed.

Applicant also respectfully points out the arguments made above with respect to at least some of the other independent claims which clearly show that Rivard does not meet applicant's specific claim language.

In addition, with respect to Claim 28, the Examiner has failed to even address applicant's claimed "receiving additional instructions from the video memory in response to the instruction request utilizing the texture module." Applicant respectfully points out the arguments made above with respect to at least some of the other independent claims which clearly show that Rivard does not meet applicant's specific claim language.

Furthermore, with respect to independent Claim 29, the Examiner has relied on Figure 6 and Figure 10 from Rivard, along with Fig. 3 from AAPA to make a prior art showing of applicant's claimed "sending an instruction request to video memory, where a texture module coupled to the shader module sends the instruction request to the video memory."

Applicant respectfully asserts that the figures relied on by the Examiner only generally illustrate a computer system and a block diagram detailing graphics accelerator system showing the pipeline latency elements 1025. In addition, in Col. 7, lines 4-7, Rivard teaches that "graphics accelerator system 635 includes pipeline latency elements 1025 to coordinate arrival of the memory data and of the associated instructions at cache data store and memory data resolver 1030" (emphasis added). Furthermore, Rivard teaches that "[m]emory request generator 1020 generates memory requests for all misses (up to four for bi-linear sampling and up to eight for tri-linear sampling), and forwards the requests..." (Col. 6, lines 50 – 52 emphasis added). However, disclosing that memory requests are generated for all misses fails to suggest "sending an instruction request to memory utilizing a texture module coupled to the shader module" (emphasis added), as claimed by applicant.

In addition, applicant respectfully asserts that Fig. 3 from AAPA as relied upon by the Examiner merely discloses that "the texels resulting from one texture lookup can

influence the location of the texels in a subsequent texture lookup" (Page 4, lines 30-31 – emphasis added). However, the mere disclosure of texels resulting from a texture lookup fail to even suggest "sending an instruction request to video memory, where a texture module coupled to the shader module sends the instruction request to the video memory" (emphasis added), as claimed by applicant. Clearly, retrieving texels from a texture lookup fails to meet "an instruction request," in the manner as claimed by applicant.

Also, with respect to independent Claim 29, applicant respectfully asserts that the Examiner has failed to even address applicant's claimed "receiving additional instructions from the video memory in response to the instruction request utilizing the texture module." Applicant respectfully asserts that, for substantially the same reasons as those argued above with respect to at least some of the independent claims, Rivard fails to even suggest any sort of additional instructions, let alone specifically "receiving additional instructions from the video memory in response to the instruction request utilizing the texture module," as applicant claims.

Applicant respectfully asserts that at least the first and third elements of the *prima facie* case of obviousness have not been met, since it would be *unobvious* to modify the Rivard reference, as noted above, and since the Rivard reference fails to teach or suggest all of the claim limitations, as noted above.

Applicant further notes that the prior art is also deficient with respect to the dependent claims. For example, with respect to Claim 18, the Examiner has relied on Figures 6 and 10, along with Col. 7, lines 4-7 from Rivard to make a prior art showing of applicant's claimed technique "wherein a complete instruction set is received in response to the instruction request."

Applicant respectfully asserts that the figures relied on by the Examiner generally illustrate a computer system and a block diagram detailing the graphics accelerator system showing the pipeline latency elements 1025. In addition, the excerpt relied on by the Examiner merely teaches that the "graphics accelerator system 635 includes pipeline

latency elements 1025 to coordinate arrival of the memory data and of the associated instructions at cache data store and memory data resolver 1030" (Col. 7, lines 4-7 - emphasis added). However, including "pipeline latency elements 1025 to coordinate arrival of the memory data and of the associated instructions" (emphasis added), as in Rivard, fails to suggest that "a complete instruction set is received in response to the instruction request" (emphasis added), as claimed by applicant. Furthermore, applicant once again respectfully asserts that Rivard actually *teaches away* from applicant's claimed technique since the "pipeline latency elements 1025" disclosed in Rivard are for the specific purpose of coordinating the arrival of the instructions and the memory data from separate sources.

In addition, with respect to Claim 19, the Examiner has relied on Figures 6 and 10, along with Col. 7, lines 4-7 from Rivard to make a prior art showing of applicant's claimed technique "wherein a partial instruction set is received in response to the instruction request."

Applicant respectfully asserts that the figures relied on by the Examiner generally illustrate a computer system and a block diagram detailing the graphics accelerator system showing the pipeline latency elements 1025. In addition, the excerpt relied on by the Examiner merely teaches that "graphics accelerator system 635 includes pipeline latency elements 1025 to coordinate arrival of the memory data and of the associated instructions at cache data store and memory data resolver 1030" (Col. 7, lines 4-7 - emphasis added). However, including "pipeline latency elements 1025 to coordinate arrival of the memory data and of the associated instructions" (emphasis added), as in Rivard, fails to suggest that "a partial instruction set is received in response to the instruction request" (emphasis added), as claimed by applicant. Furthermore, applicant once again asserts that Rivard actually *teaches away* from applicant's claimed technique since the "pipeline latency elements 1025" in Rivard are for the specific purpose of coordinating the arrival of the instructions and the memory data from separate sources.

Again, since at least the first and third element of the *prima facie* case of obviousness have not been met by the Rivard reference, as noted above, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

To this end, all of the independent claims are deemed allowable. Moreover, the remaining dependent claims are further deemed allowable, in view of their dependence on such independent claims.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. NVIDP064/P000286).

Respectfully submitted,
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